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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

DUONG, THOI V

ART UNIT	PAPER NUMBER
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2871

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/852,647

Applicant(s)

JUN, SAHNG-IK

Examiner

Thoi V Duong

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 October 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-35 ~~is~~/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10-34 ~~is~~/are allowed.
- 6) ☒ Claim(s) 1-9 and 35-38 ~~is~~/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 27, 2004 has been entered.

Accordingly, claims 1 and 35 were amended. Currently, claims 1-35 are pending in this application.

Claim Objections

2. Claim 1 is objected to because of the following informalities: claim 1 recites the limitation "the same layer" in line 7. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

3. Claim 35 is objected to because of the following informalities: claim 35 recites the limitation "the same layer" in line 5. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application

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by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 35-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Fukuda (USPN 6,746,905 B1).

Re claim 35, as shown in Figs. 4A and 4B, Fukuda discloses a liquid crystal display, comprising:

- a gate line 42 formed on a substrate 11;

- a data line 41 insulated from and intersecting said gate line;

- a semiconductor layer comprising a semiconductor pattern 12 and a light interception pattern 62 formed on the substrate 11 as shown in Fig. 9 (col. 5, lines 37-41 and col. 13, lines 24-35);

- a thin film transistor connected to said gate line and said data line, said thin film transistor including the semiconductor pattern; and

- a field-generating electrode 32 having a portion laterally spaced apart from said data line with a gap therebetween,

- wherein the semiconductor layer comprising the light interception pattern overlaps the gap (Fig. 4B);

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wherein, re claim 36, said light interception pattern and said data line overlap each other, and said light interception pattern and said field-generating electrode overlap each other (Fig. 4B);

wherein, re claim 37, the semiconductor layer is connected to said light interception pattern (col. 13, lines 36-43); and

wherein, re claim 38, said light interception pattern included in the semiconductor film is wider than said data line 41 (Fig. 4A).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuda (USPN 6,746,905 B1) in view of Yamazaki et al. (USPN 5,892,562).

Re claim 1, as shown in Figs. 4A and 4B, Fukuda discloses a liquid crystal display, comprising:

a plurality of gate lines 42 formed on a substrate 11;

a plurality of data lines 41 insulated from and crossing over said plurality of gate lines;

a plurality of pixel regions defined by the crossing of said plurality of gate lines and said plurality of data lines (Fig. 4A);

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a semiconductor layer comprising a semiconductor pattern 12 and a light interception pattern 63 formed on the substrate 11 as shown in Fig. 9 (col. 5, lines 37-41 and col. 13, lines 24-35);

a pixel electrode 32 formed in each pixel region; and

a thin film transistor provided to each pixel region and including the semiconductor pattern,

wherein, re claim 2, as shown in Fig. 4B, said light interception pattern included in the semiconductor film and said data line 41 corresponding thereto overlap each other, and said light interception pattern and said pixel electrode 32 close to said data line corresponding thereto overlap each other;

wherein, re claim 4, the semiconductor pattern 12 is connected to said light interception pattern corresponding thereto (col. 13, lines 36-43);

wherein, re claim 5, the semiconductor pattern is extended to said data line corresponding thereto (Fig. 4B);

wherein, re claim 6, the light interception pattern 63 is extended beyond a periphery of said data line corresponding thereto (Fig. 4A); and

wherein, re claim 8, said pixel electrode 32 is formed on the same plane as said plurality of data lines 41 (Fig. 4B).

wherein, re claim 9, as shown in Fig. 10, pixel electrode 22 is formed on the plane different from said plurality of data lines 41; and

wherein, re claim 3, said light interception pattern 63 and pixel electrode 32 overlap each other (Fig. 4B).

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Fukuda discloses a liquid crystal display device that is basically the same as that recited in claims 1 and 7 except for a common electrode spaced apart from the pixel electrode with a predetermined distance and formed on the same plane as said plurality of gate lines

As shown in Figs. 6 and 7A, Yamazaki et al. also discloses a common electrode 609 formed on the same plane as a plurality of gate lines 608 and a pixel electrode 625 spaced apart from the common electrode 609 with a predetermined distance.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the liquid crystal display of Fukuda with the teaching of Yamazaki et al. by employing an electrode structure having a common electrode formed on the same plane as the plurality of gate lines and spaced apart from the pixel electrode with a predetermined distance so as to minimize noncontinuity of the electric field strength around each pixel electrode and improve the display characteristics (col. 3, lines 18-23).

Allowable Subject Matter

8. Claims 10-34 are allowed.

The following is an examiner's statement of reasons for allowance: none of the prior art of record fairly suggests or shows all of the limitations as claimed. Specifically,

Re claims 10 and 22, none of the prior art of record discloses, in combination with other limitations as claimed, a liquid crystal display (as well as a method of fabricating the same) comprising a light interception pattern formed of the same material as said semiconductor pattern on the gate insulating layer.

The most relevant references, USPN 6,466,289 B1 of Lee et al. and USPN 5,247,289 of Matsueda, fail to disclose or suggest a semiconductor layer comprising a semiconductor pattern and a light interception pattern or a light interception pattern formed of the same material as said semiconductor pattern on the gate insulating layer. As shown in Figs. 3, 6 and 7, the reference of Lee et al. discloses a light interception pattern 64 and a semiconductor pattern 40 formed on the gate insulating layer 30; however, the material of the light interception pattern 64 is different from that of the semiconductor pattern 40 (col. 3, lines 33-34 and 54-56). Meanwhile, as shown in Fig. 7, the Matsueda's reference discloses a semiconductor portion formed of the same layer as a semiconductor pattern 78 on top of a common electrode 81; however, this semiconductor portion does not function as a light interception pattern. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

9. Applicant's arguments filed October 27, 2004 have been fully considered but they are not persuasive.

Applicant argued that Fukuda and Yamazaki fail to disclose a semiconductor layer comprising a semiconductor pattern and a light interception pattern formed on the same layer. However, the limitation "formed on the same layer" recited claims 1 and 35 has not given patentable weight since there is insufficient antecedent basis for this

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limitation. It is also noted that the reference of Lee as indicated in Applicant's remarks was not cited in the last office action. Finally, Yamazaki is employed for teaching an in-plane LCD device where a common electrode is formed on the same plane as a plurality of gate lines and spaced apart from a pixel electrode with a predetermined distance.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (571) 272-2293.

Thoi Duong



12/31/2004



TARIFUR R. CHOWDHURY
PRIMARY EXAMINER